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COMPARISON OF THE REDUCED NUMBER OF SWITCHING ELEMENTS MULTILEVEL INVERTERS

Abdulvehhab Kazdaloglu[*1], Bekir Cakir[2], Kutay Is[3] & Aziz Guneroglu[4]
[*1,2,3&4]Department of Electrical Engineering, Faculty of Engineering, Kocaeli University, Kocaeli, Turkey

ABSTRACT
In this study, the multi-level inverter is supplied with asymmetric sources, the output voltage wave patterns of change were examined. Also, unlike other applications in the literature R (resistive) load, except RL (resistive-inductive) that may be in the form of output voltage waveforms in case of load changes are examined.

Keywords: *Inverter, multilevel, symmetric, asymmetric, load.*

I. INTRODUCTION

Multilevel inverters, has attracted first developed in 1924 by Erwin Marx and attention with a high voltage circuit known as the Marx generator. As a result of studies of the mathematical modeling of Multilevel inverter systems is easier to do the simulation of Inverters[1,2]. The objective of multilevel inverters is increasing the number of levels to obtain a voltage waveform close to pure sinusoidal. For this purpose, a number of studies have been made [3].

When the number of inverter level is increased, the output voltage is close to the sine shape and thus inverter can feed more sensitive loads, such as induction motor drives [4]. Multilevel inverters are used to connect the renewable energy sources producing DC voltage to the network. [5]. Unlike the Traditional multi-level inverter topologies the new topologies can be seen in the literature One of these new topologies is the asymmetrical hybrid multilevel inverter topology. This topology is obtained by using H-Bridge with three known topologies (diode clamping, flying capasitor is, cascade) [6].
One of the main problems of multilevel inverters is contain a large number of switching elements and the difficulty of controlling these components. For this purpose, studies for reducing the number of the switching element have been made [7].
In this study,multi-level inverter topology is obtained by reducing the number of switching elements compared in different feeding conditions and at different load conditions, and the results was investigated.

II. THE COMPARISON OF INVERTER TOPOLOGIES, FOR SYMMETRIC AND ASYMMETRIC FEEDING CONDITION

In the literature a lot of multi-level inverter topologies, such as Diode clamped, Capacitor clamped (flying capasitor) and H-bridge, are recommended. Here, we will examine the cascaded H bridge topology applications, which are reduced the number of switching element.

the symmetric and asymmetric multilevel inverters supply situation and resistive R (38Ω), ohmic-inductive and RL (R = 38Ω L = 28mh) load cases were examined below.

A. Topology 1

Topology applied to reduce the number of switching elements is shown in Figure 1. In the figure, S1 and S3 unidirectional switching elements, the switching element S2 is bidirectional. S2 switch blocking voltage while providing bidirectional current flow [8].

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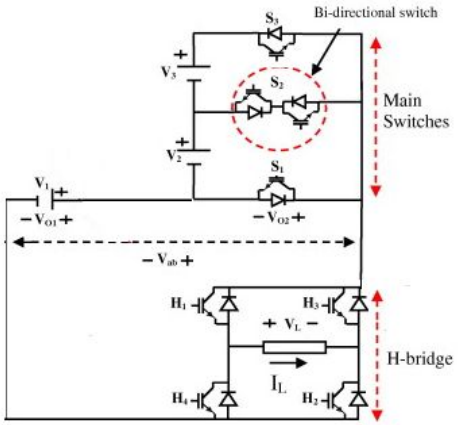

Figure 1: New topology obtained by reducing the number of switching elements [8]

$$V_{max}=V_1+V_2+V_3 \quad (1)$$

When the Circuit topology is simulated under R (38Ω) and RL (R = 38Ω L = 28mh) load. The Output voltage and current waveforms are shown. The harmonic distortion of voltage and current values occur under this load (VTHD, Ithd) is given under the figures.

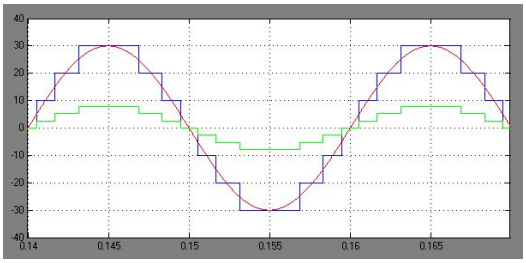

Figure 2: Reduced the number of switching element 7 level inverter output voltage and current waveforms with R load. $V_{THD}=I_{THD}=12\%$

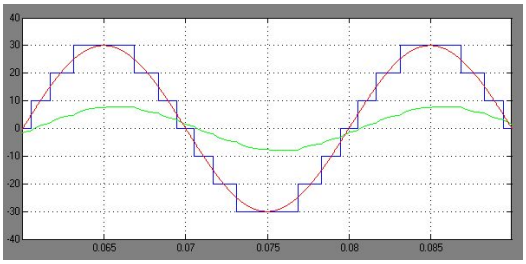

Figure 3: Reduced the number of switching element 7 level inverter output voltage and current waveforms with RL load, $V_{THD}=12\%$ $I_{THD}=3.5\%$

If we use an asymmetric feed for the same topology, theoretical, output level reaches 13. But in this topology, the feed situation of asymmetric source V1 will be activated in any case is not suitable for this topology. For 13 level status; Level 1, Level 3 and Level 6 is formed in positive alternans . Due to the nature of the topology, the 2, 4 and 5 levels are not formed. the fact that instead of the 13-level inverter for asymmetric supply situation is realized as 6 levels. Asymmetrical multilevel inverter-fed output voltage and current waveforms in the case of variable load are shown below.

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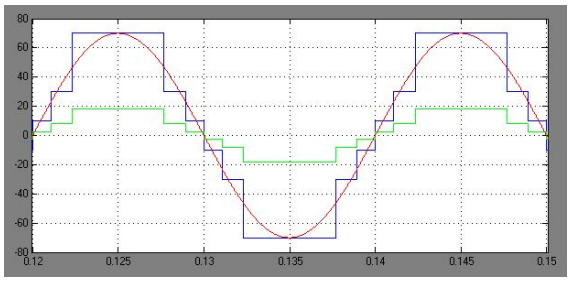

Figure 4: Reduced the number of switching element 7 level inverter output voltage and current waveforms with R load. V_{THD}=I_{THD}=16%

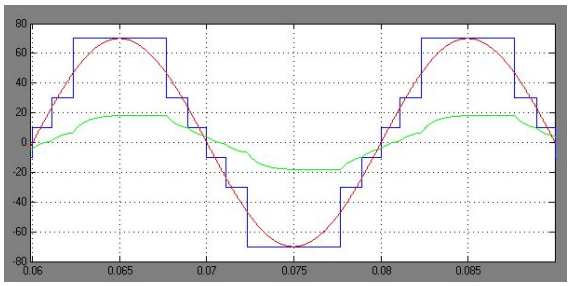

Figure 5: Reduced the number of switching element 7 level inverter output voltage and current waveforms with RL load, V_{THD}=16% I_{THD}=7%

B. Topology 2

A symmetrically fed 7-level inverter topology, applied to reduce number of switching elements, is given in figure6 [9]. 6 IGBTs are used in this topology as the switching element. For the Inverter topology is given in Figure 6, the output voltage waveform, the voltage waveform transmission ranges of IGBTs and IGBT drive circuits for the formation of the output voltage waveforms are given in Figure 7-8-9-10.

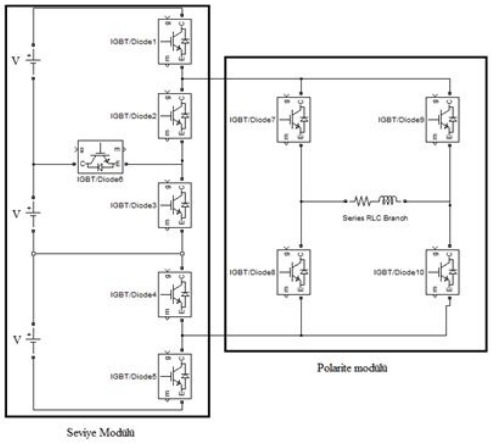

Figure 6 : Symmetrically fed 7-level inverter topology [9]

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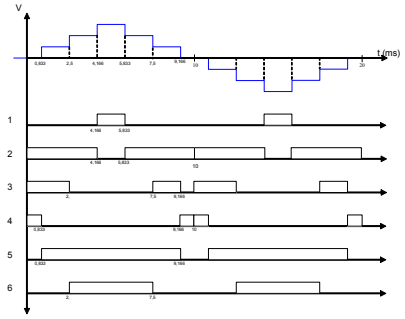


Figure 7: 7-level inverter output voltage waveform for the IGBT conduction conditions. [9]

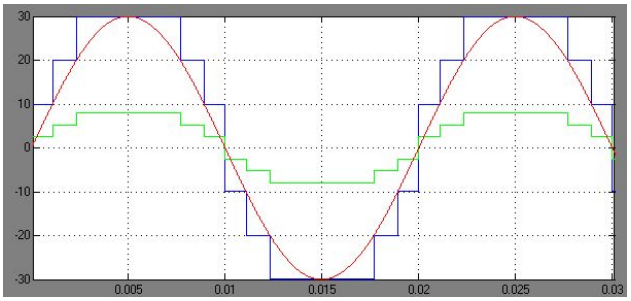


Figure 8: 7-level inverter output voltage and current waveforms with R load, V_{THD}= I_{THD}=17%

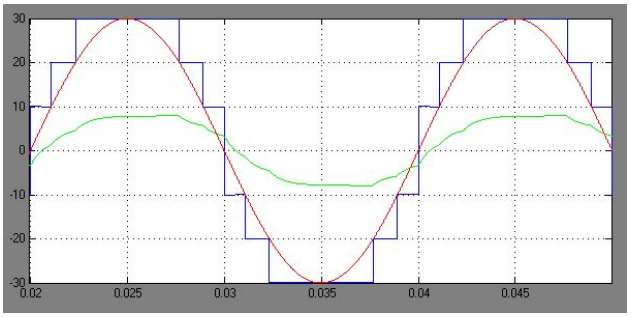
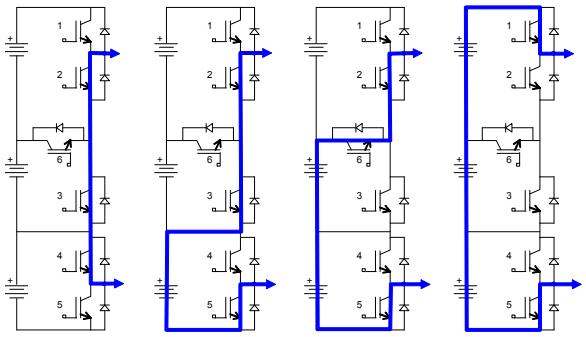


Figure 9: 7-level inverter output voltage and current waveforms with RL load, V_{THD}=17% I_{THD}=10%



a b c d

Figure 10: a) The inverter output 0 level. (2 - 3 - 4 IGBTs transmission condition).
b) The inverter output 1 level (2 – 3 – 5 IGBTs transmission condition)
c) The inverter output 2 level (2 – 6 – 5 IGBTs transmission condition)
d) The inverter output 3 level (1 – 5 IGBTs transmission condition) [9]

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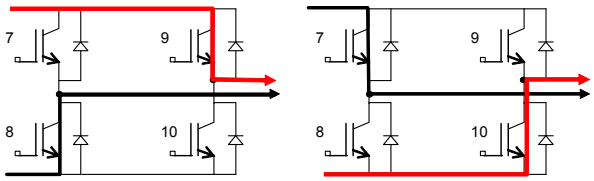
The important point to note here, the 2 IGBT that control each voltage source should not transmit at the same time. For each case, Only one of 2 IGBTs is in transmission condition. In addition, The output voltage polarity of this inverter topology is controlled by a separate H-bridge IGBTs group. H-bridge IGBT group and IGBTs conduction conditions are given in figure 11.



a b

Figure 11: a)Inverter output + (8 – 9 5 IGBTs transmission condition)
b) Inverter output – (7 –5 IGBTs transmission condition)[9]

If we use an asymmetric feed for the same topology, theoretical, output level reaches 15. switching states for the 15 level is; IGBT switching states of the expulsion of Table 1 are met taking into account the output voltage and current waveforms occur is given in Figure 12-13.

TABLE 1: Possible switching states for the state of the asymmetric feeding

Output Level	IGBTs With Transmission
0	2-3-4
1	2-3-5
2	2-6-4
3	2-6-5
4	1-6-3-4
5	1-6-3-5
6	1-4
7	1-5

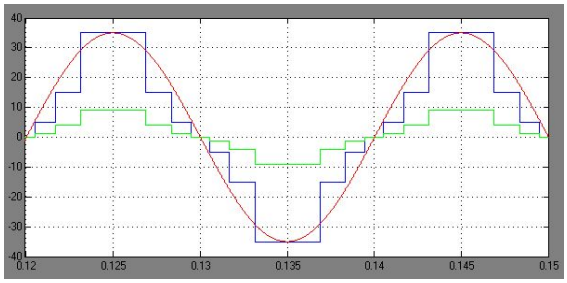


Figure 12: The asymmetric feeding ouput voltage and current waveforms with R load, V_{THD}= I_{THD}=27%

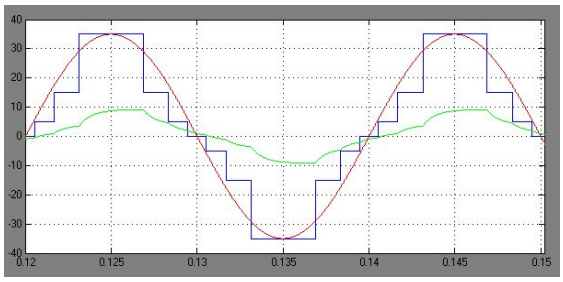


Figure 13: The asymmetric feeding ouput voltage and current waveforms with RL load, V_{THD}=27% I_{THD}=18%

In case of asymmetric feed, the 4, 5 and 6 level does not occur. after the 3rd Level, is skipped to 7th level. In this case the voltage output is out in the form of sine .

C. Topolgy 3

In this topology without changing the number of switch, If the place of IGBTs changes, a topology for asymmetric feeding will be obtained. If the IGBT-6 location is changed and connected in series with the indicated source of 2V, this problem will be eliminated. The topology is obtained by changing the position of the IGBT-6 is shown in Figure 14.

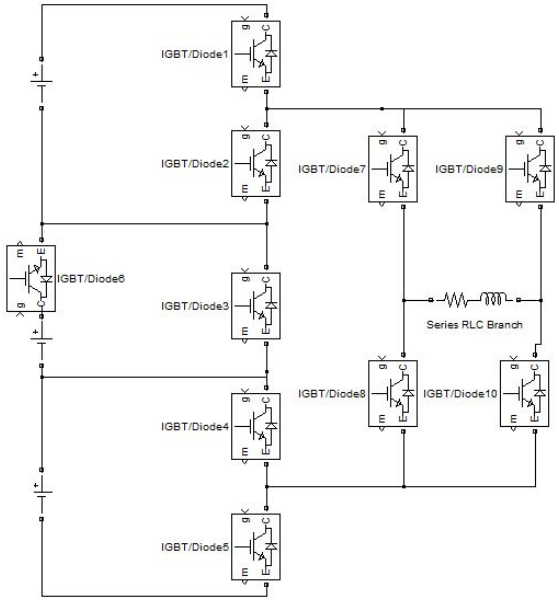


Figure 14: inverter topology for symmetric and asymmetric feeding

If the feed of the inverter's used in this topology sources is selected in equal size (symmetric) , the output will be 7 levels.

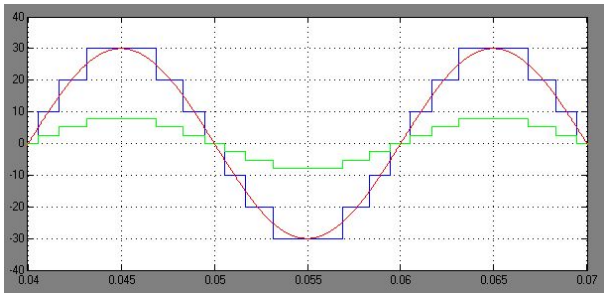


Figure 15: The symmetric feeding ouput voltage and current waveforms with R load, V_{THD}= I_{THD}=12%

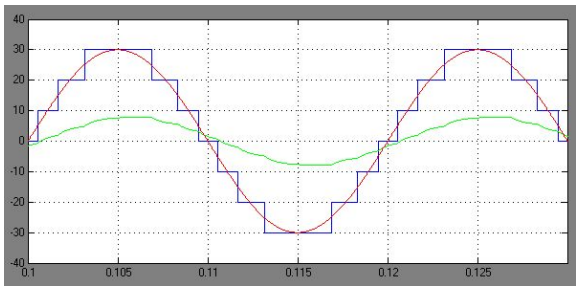


Figure 16:The symmetric feeding ouput voltage and current waveforms with RL load, V_{THD}=12% I_{THD}=3%

If asymmetric (2n, 1-2-4 as the exponent multiples of 2) is selected, the output will be 15 levels. Simulation results for the asymmetric feeding situation in the same topology are given below.

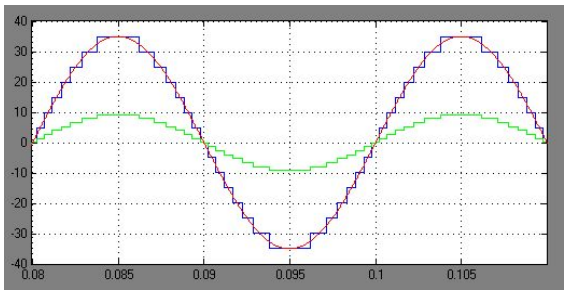


Figure 17: Asymmetric feeding 15 level inverter topology output voltage and current waveforms with R load, V_{THD}= I_{THD}=5.5%

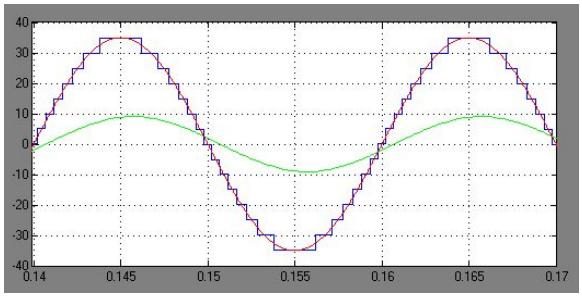


Figure 18: Asymmetric feeding 15 level inverter topology output voltage and current waveforms with RL load, V_{THD}=5.5% I_{THD}=1%

D. Topolgy 4

Using Diode instead of IGBTs connected in parallel to the resources of DC was obtained the 15 simplified multi-level inverter topologies are also available. [10]. But these studies, only R (resistive) load is specified for the ideal. The simulation results are given below for Asymmetric supply situation in the same topology.

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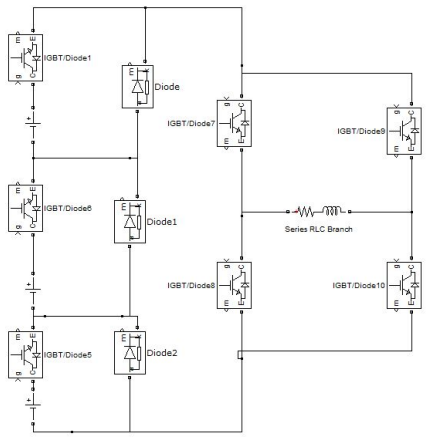

Figure 19: İnverter topology for symmetric and asymmetric feeding

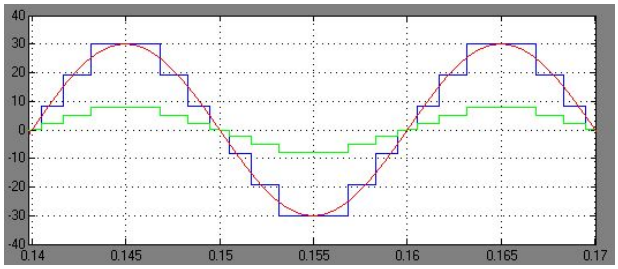

Figure 20: The symmetric feeding ouput voltage and current waveforms with R load, V_{THD}= I_{THD}=13%

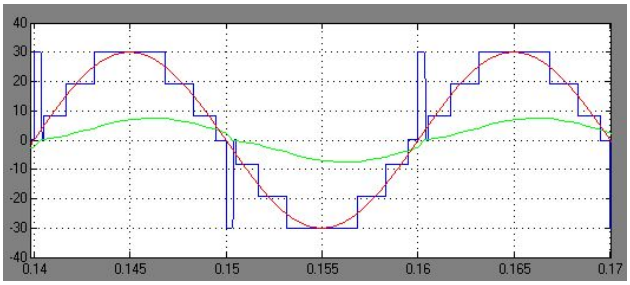

Figure 21: The symmetric feeding ouput voltage and current waveforms with RL load, V_{THD}=27% I_{THD}=8%

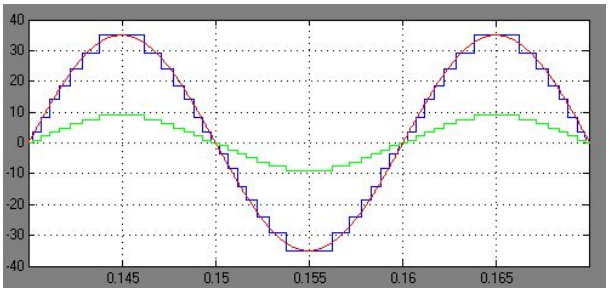

Figure 22: Asymmetric feeding 15 level inverter topology output voltage and current waveforms with R load, V_{THD}= I_{THD}=6%

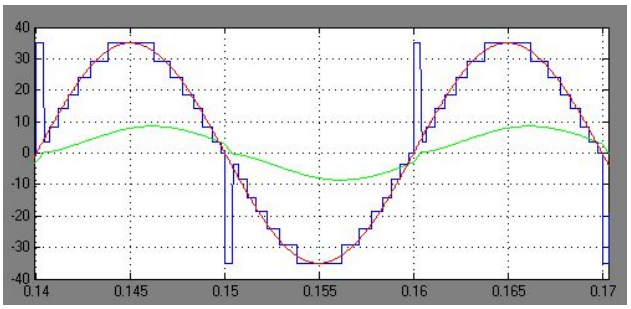

Figure 23: Asymmetric feeding 15 level inverter topology output voltage and current waveforms with RL load, V_{THD}=26% I_{THD}=7%

III. CONCLUSION

In this study, reduced the number of switching elements of multi-level inverter output voltage and current waveforms change with different feed voltages and different load cases were examined. The objective of multilevel inverters, as far as possible the output the approximation is to pure sine shape therefore minimize the ITHD and VTHD. Firstly, the number of switching elements in the literature topologies were compared according to different feeding conditions and situations to work in different load conditions. The comparison results are given in table 2.

Table 2: Inverter topologies according to the comparison of symmetric-asymmetrik feeding and RL load.

Topology	Number of IGBT	Number of Diode	Symmetric Feeding	Asymmetric Feeding	R-L load
1	4	-	✓	X	✓
2	6	-	✓	X	✓
3	6	-	✓	✓	✓
4	3	3	✓	X	X

Subsequently, the ITHD and VTHD values are compared for the investigated topologies. The resulting values of Table 3 were obtained.

Table 3: Inverter topologies according to the comparison of symmetric-asimerik feeding and total harmonic distortion with R and Rl load

Feeding	**Topology**	**Level**	**R**		**RL**	
			V_{THD}	**I_{THD}**	**V_{THD}**	**I_{THD}**
Symmetric	1	7	12	12	12	3,5
	2	7	17	17	17	10
	3	7	12	12	12	3
	4	7	13	13	27	8
Asymmetric	1	7	16	16	16	7
	2	7	27	27	27	18
	3	**15**	**5,5**	**5,5**	**5,5**	**1**
	4	15	6	6	26	7

*ITHD and VTHD values in the table are given in %

As a result of simulation studies for 4 topology examined in this study, The 3rd topology called MultiSource Topology in the literature is found to be the optimal topology for symmetrical-asymmetrical feed conditions and variable load conditions. Simulations conducted for this topology, the ITHD value IEEE1547 standard, well below 5% occurred in 1%

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